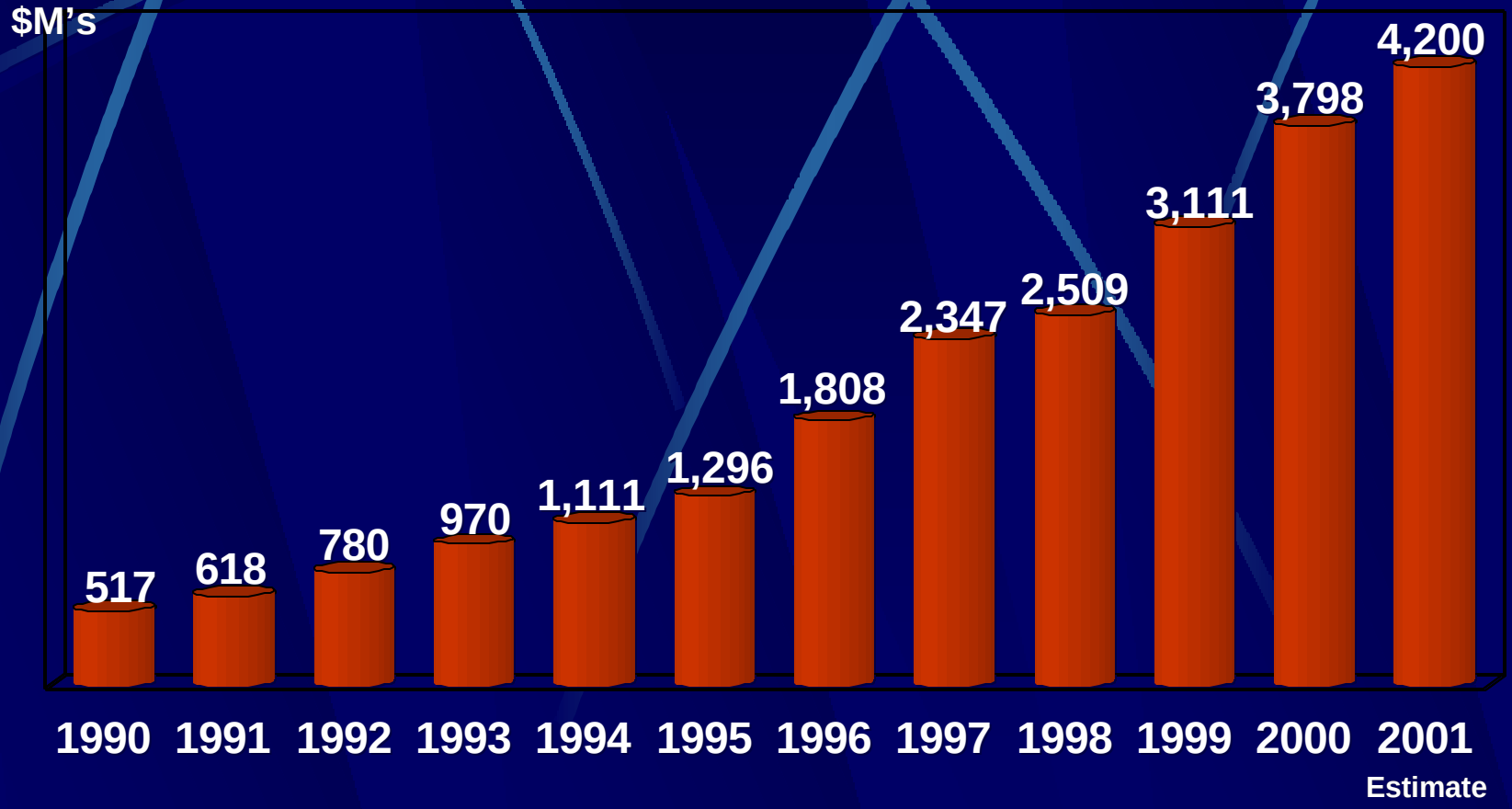
Intel Research & Development
RP1 lab

Dr. Gerald Marcyk
Director, Components Research
Logic Technology Development

Increasing Commitment to Research & Development



Source: Intel 2001 Annual Report

Over 6,000 Scientists and Technologists Worldwide

Marcyk May 2001

Specializing in a Number of Technical Disciplines

INTERNET

- Connecting business professionals
- Connecting consumers
- Building the new internet infrastructure

ITU

G. Lite
H. 263
v. 90

COMMUNICATIONS

- Networking
- Cellular

COMPUTING

- Architecture and platform improvements

USB
UNIVERSAL SERIAL BUS

W3C

XML
SMIL

SILICON AND MANUFACTURING

- Cost effective Manufacturing
- Continuing Moore's Law
- Novel applications of Silicon

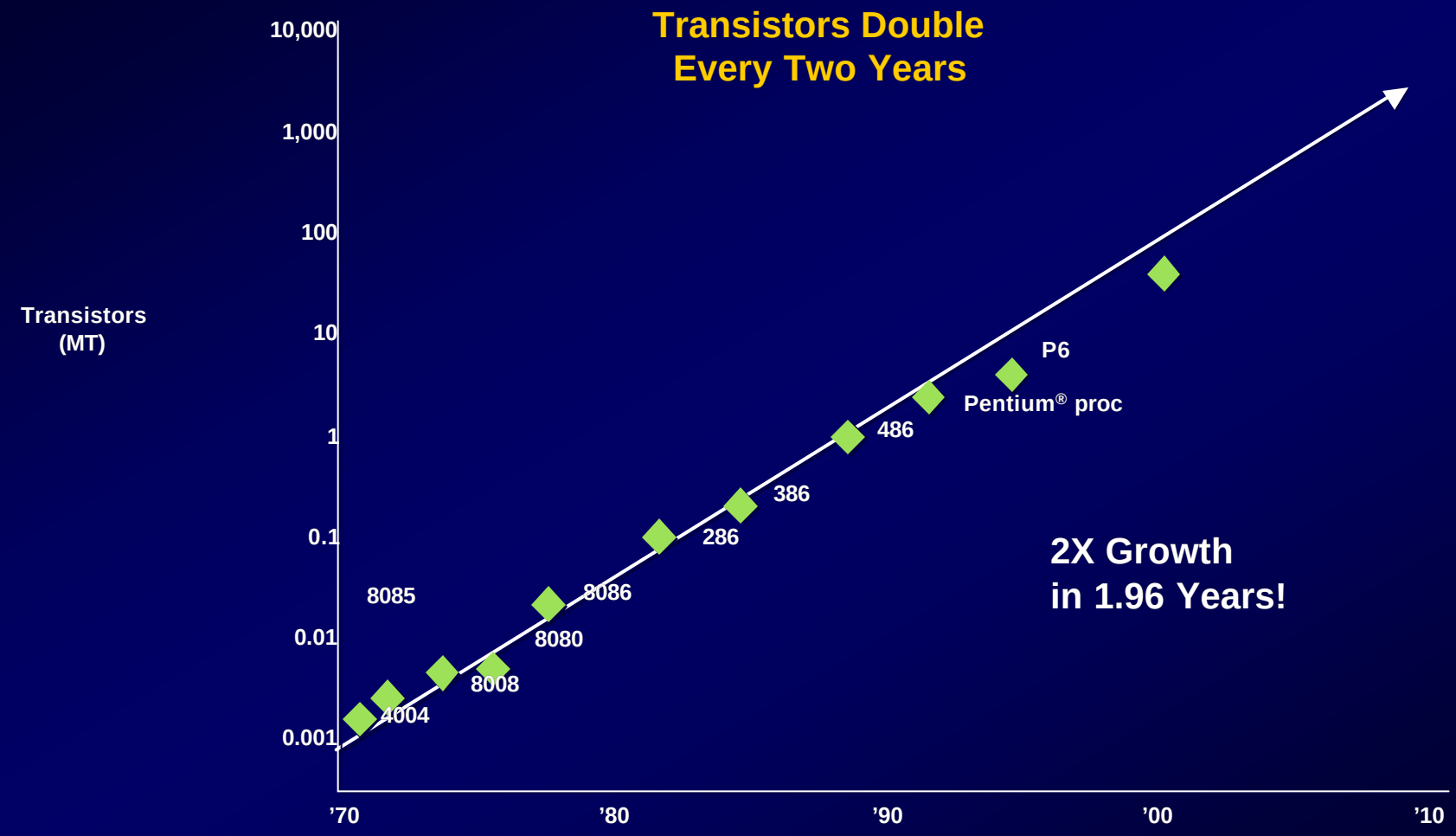
Components Research

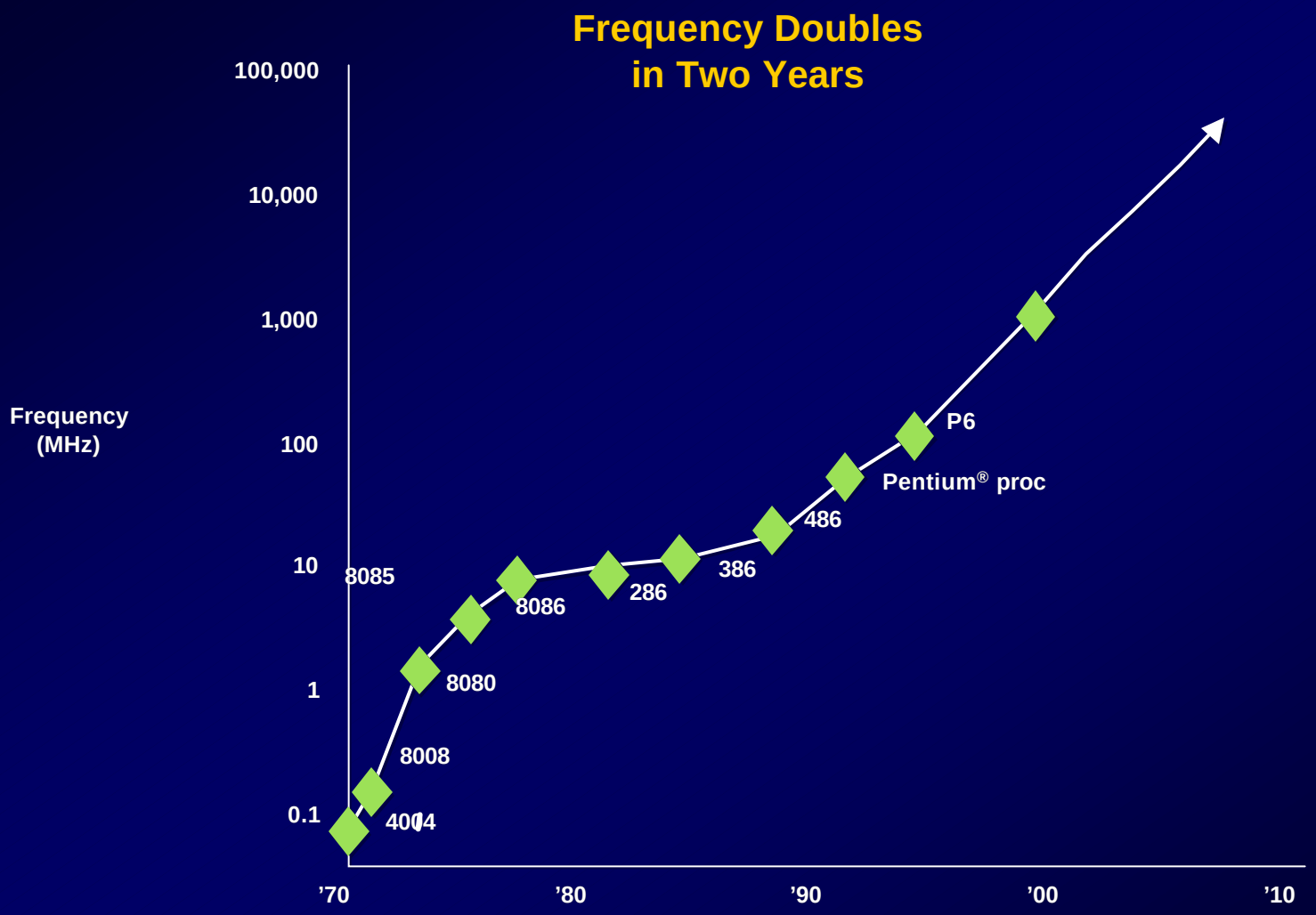
- Geographically aligned with internal development customers
- Silicon Technology
  - Hillsboro, Oregon
- Mask Making
  - Santa Clara, California
- Packaging
  - Chandler, Arizona

Moore's Law Drives Research, Development & Manufacturing

Our Goal:

- New technology generation every 2 years
  - 2x die per wafer
  - ½ transistor cost
  - 2x microprocessor speed
- Flawless ramp of new technologies into HVM
  - high yields, cost effective manufacturing
  - Copy Exactly transfer
- Introduce new products during HVM ramp
  - deliver best products on the best technology


Transistors Double
Every Two Years
Transistors
(MT)
10,000
1,000
100
10
1
0.1
0.01
0.001
4004
8008
8080
8085
8086
286
386
486
Pentium® proc
P6
2X Growth
in 1.96 Years!
'70
'80
'90
'00
'10


Frequency Doubles
in Two Years
Frequency
(MHz)
100,000
10,000
1,000
100
10
1
0.1
'70
'80
'90
'00
'10
4004
8008
8080
8085
8086
286
386
486
Pentium® proc
P6

IC Process Evolution

	Actual				Forecast			
Process Name	P854	P856	P858	Px60	P1262	P1264	P1266	P1268
1st Production	1995	1997	1999	2001	2003	2005	2007	2009
Lithography	0.35	0.25	0.18	0.13	0.10	0.07	0.050	0.0035
Gate Length	0.35	0.20	0.13	0.07	0.05	0.035	0.025	0.015

Physical Gate Length < Lithography Generation

Process Evolution

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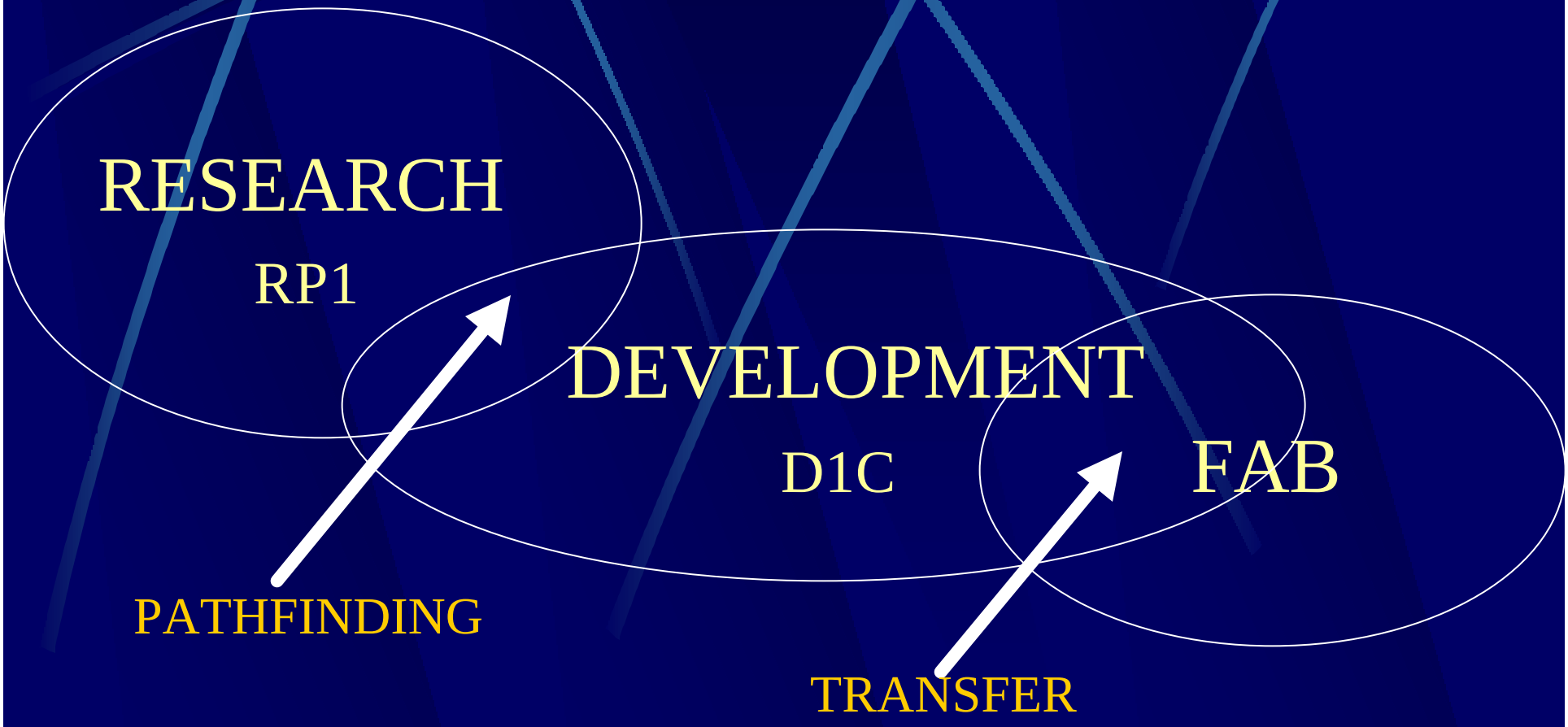
Process Evolution



Technology Evolution

- External Research: P1268 (35 nm)
  - Assess high risk and disruptive technologies
  - Fund universities and consortia
- Internal Research: P1266 (50 nm)
  - Demonstrate feasibility of new technologies
  - Joint development with suppliers
- Pathfinding: P1264 (70 nm)
  - Demonstrate new technologies in-house on 300mm
  - Make major architecture decisions
  - Performance, risk, schedule, and cost

Technology Evolution (cont.)

- Technology Development: P1262 (100nm)
  - Deliver a world class technology
  - Performance, Schedule, Cost
  - Final HVM tool selection
- Manufacturing Ramp: Px60 (0.13 μm)
  - Copy Exactly transfer to multiple fabs
  - Output, Schedule, Cost
- Maturity: P858 (0.18 μm)
  - Cost, Output, Continuous Improvement

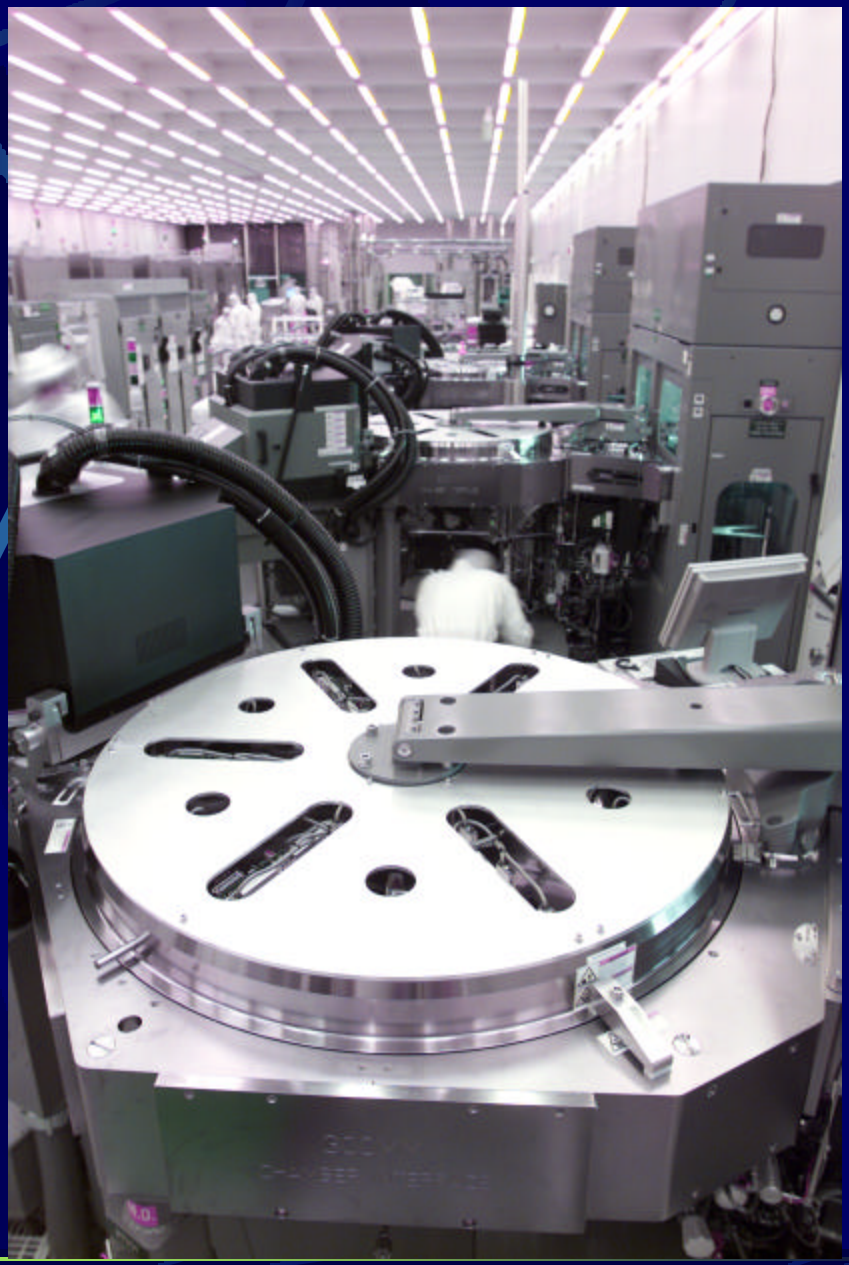
What is the Research & Pathfinding lab (RP1) ?

- World's first 300mm silicon research lab
  - 115,000 sq ft research building
    - Approx 56,000 sq ft of class 1 clean room at build-out
      - 28,000 sq ft in phase 1
    - Linked to development fabs
- Dedicated space for our most advanced silicon technologies and equipment
  - RP1 houses speculative research
  - Standard & development steps supported in D1C

RP1
From Beakers ....

RP1

to Batches ...



... To Devices

Why is RP1 important?

- Intel's silicon R&D infrastructure now fully implemented in Ronler Acres campus
  - RP1: research
  - D1C: development & transfer
  - Fab20/D1B: manufacturing
- Fully leverages our D1C Development Fab
  - Wafers can move seamlessly from research to development to manufacturing
  - Allows researchers to focus on novel ideas not standard activities
- Major commitment to silicon research in Oregon

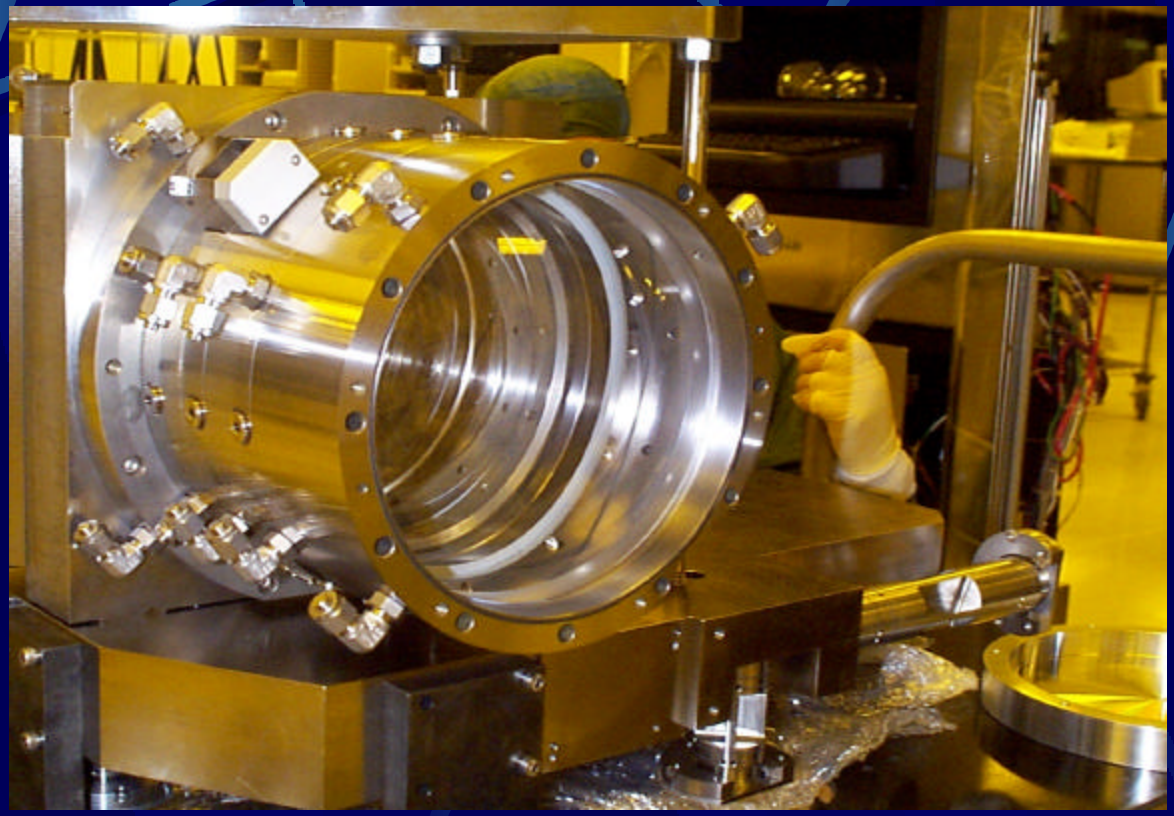
What kind of Research in RP1?

- Advanced Lithography
  - 157nm and Extreme Ultraviolet exposure tools
- Advanced Transistors
  - Home of world's smallest & fastest CMOS
- Advanced Interconnects
  - Copper and Optical
- Environmentally benign processes
  - New materials and chemistries

Lithography

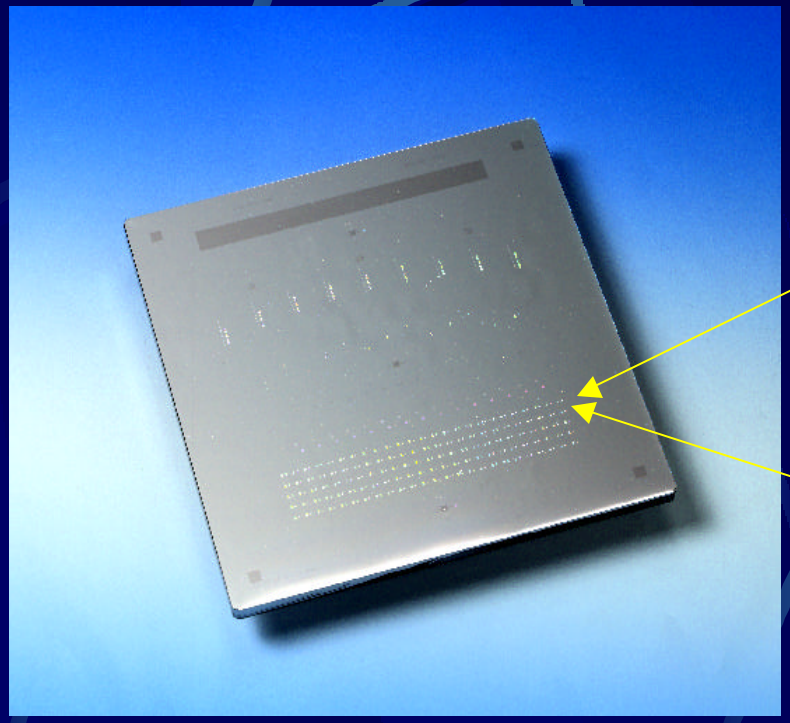
- Challenge: cost effective way to print smaller dimensions
- One Research Approach
  - Shrink wavelength of exposure light
    - 248 nm wavelength — manufacturing
    - 193 nm wavelength — development
    - 157nm wavelength — pathfinding
    - 13nm (EUV) wavelength — research

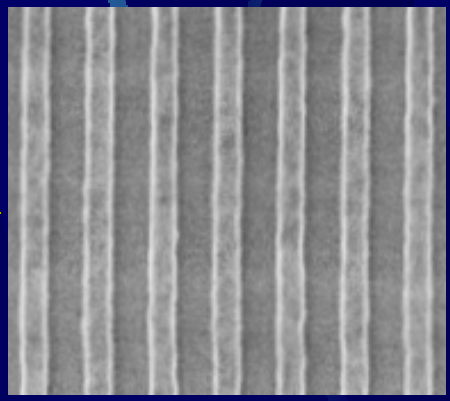
Delivery of World's First 157 nm Miniscanner



CaF_2 lens element in N_2 purged projection optics

Intel Delivers World's First 6" EUV Mask

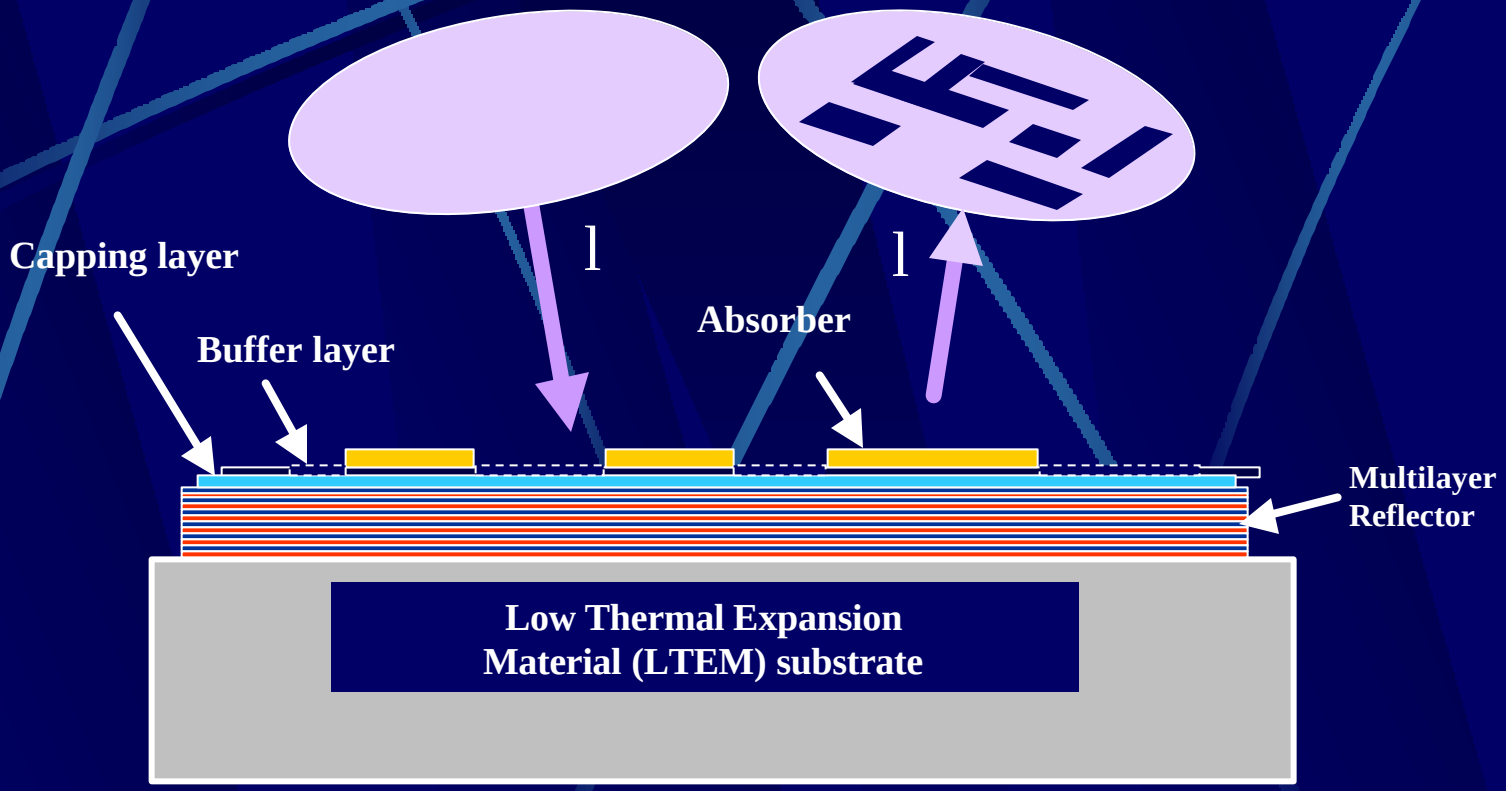




120 mm x 104 mm field size

200 nm lines/spaces for 50 nm node

EUV mask making revolution: Reflective masks

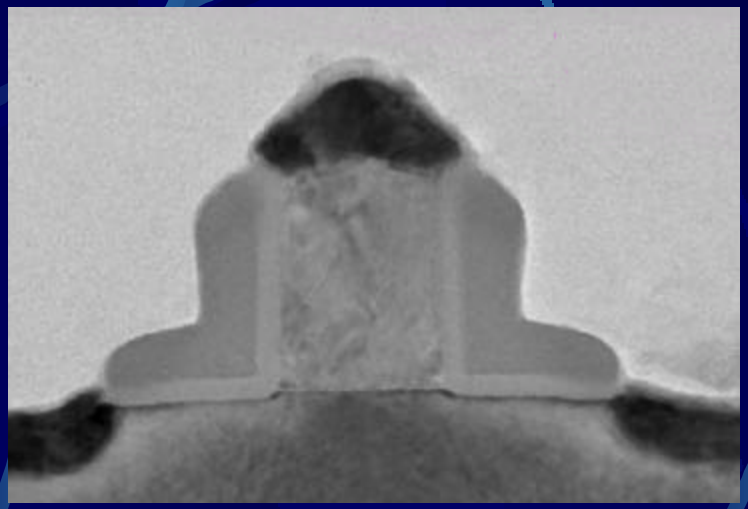


Mask structure with incident and reflected EUV light

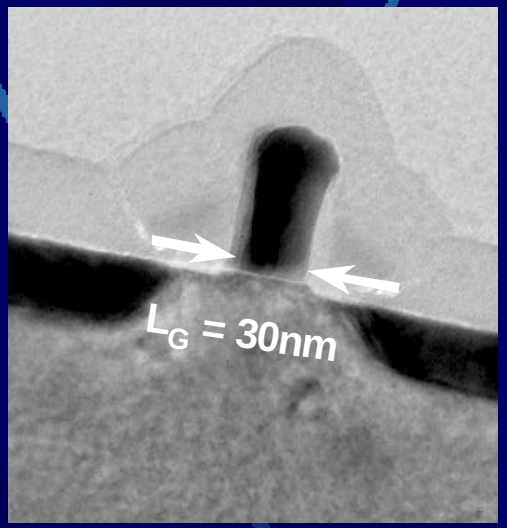
Transistors

- The engine that drives device performance
- Our goals:
  - High density
  - High performance
  - Low voltage
  - Low power

Highest Performance Transistors

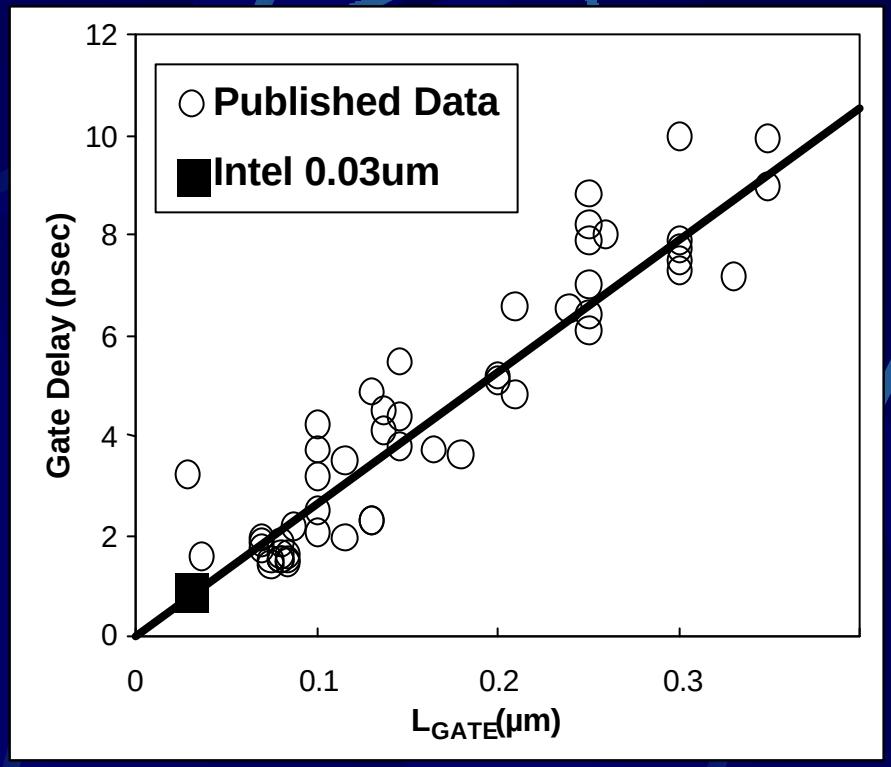


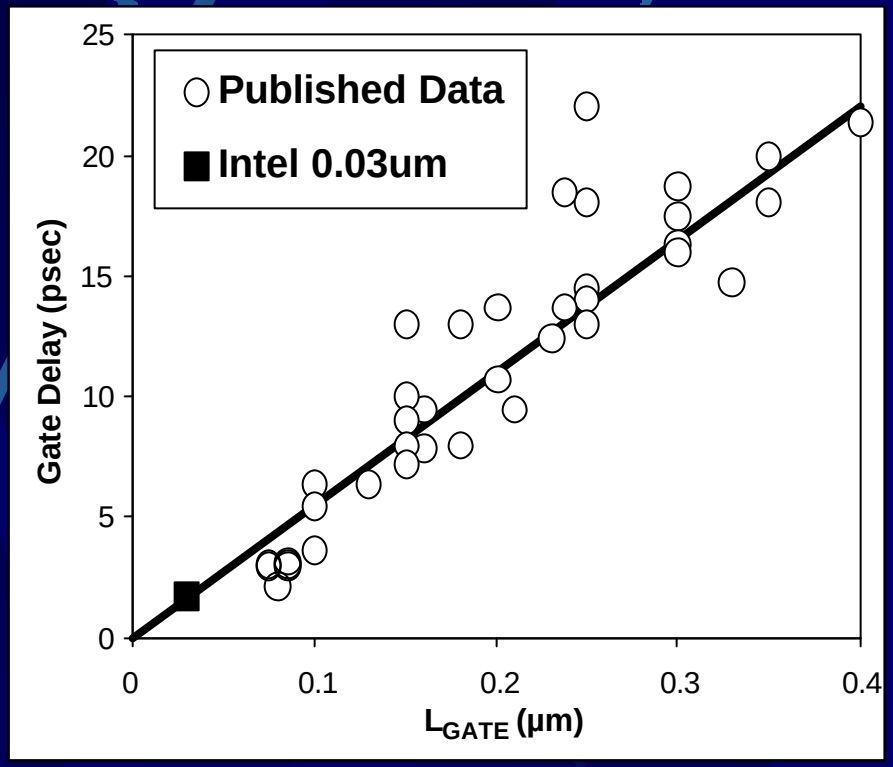
World's highest performance transistor in manufacturing: P860 Technology
0.13 mm GENERATION



Research is 2 generations ahead of manufacturing
0.07mm GENERATION

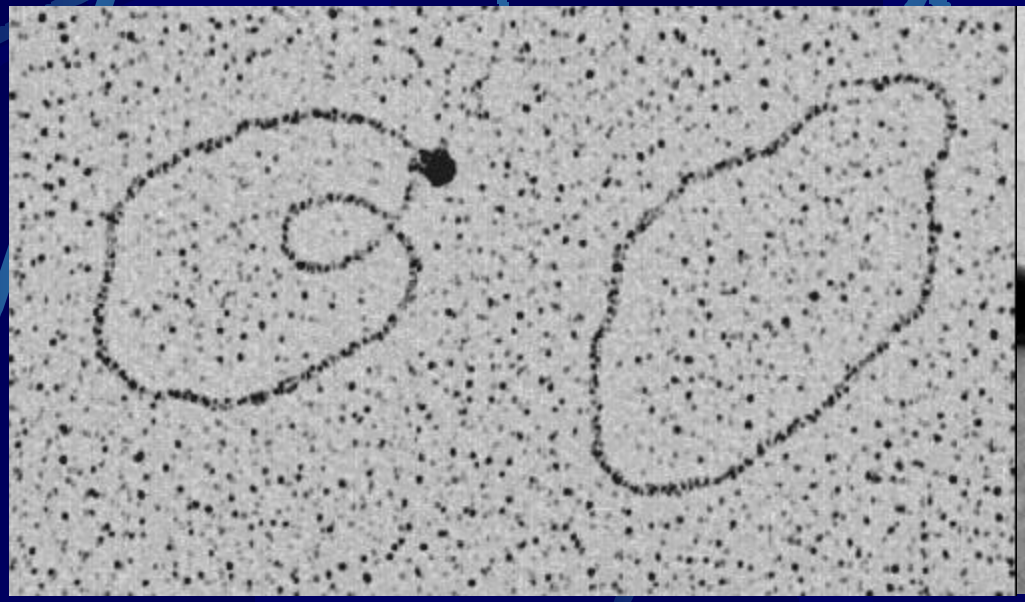
30nm Physical L_G CMOS Transistors Demonstrated with World Record Gate Delays



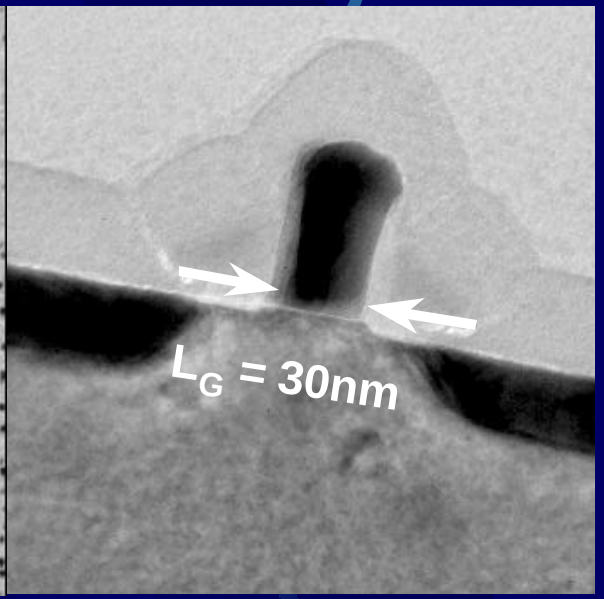


Gate delays at 0.85 volts!

Transistors as Small as DNA

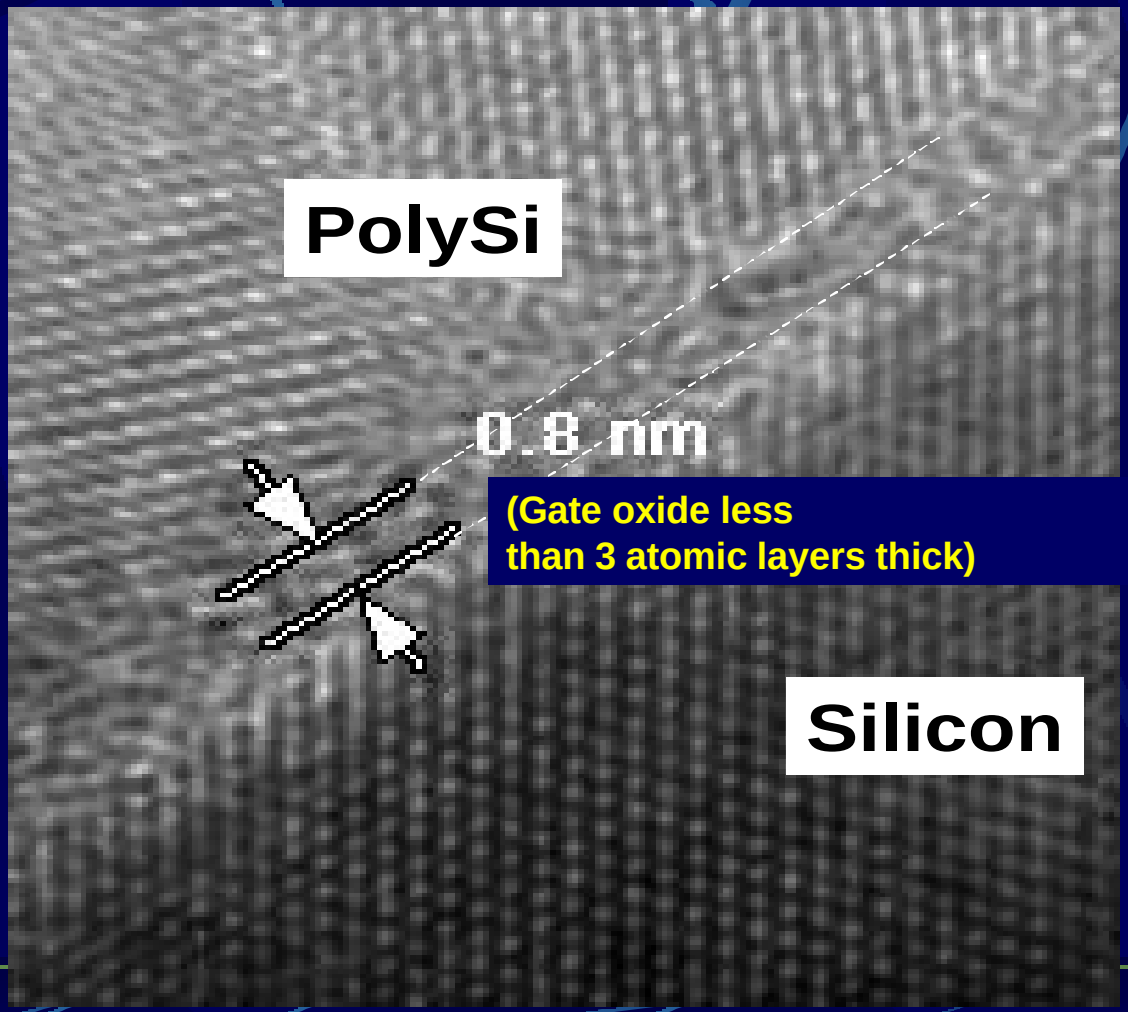


10nm Gold particle attached to Z-DNA antibody
[John Jackson & Inman. Gene 1989 84 221-226]



30nm Intel
Research Transistor

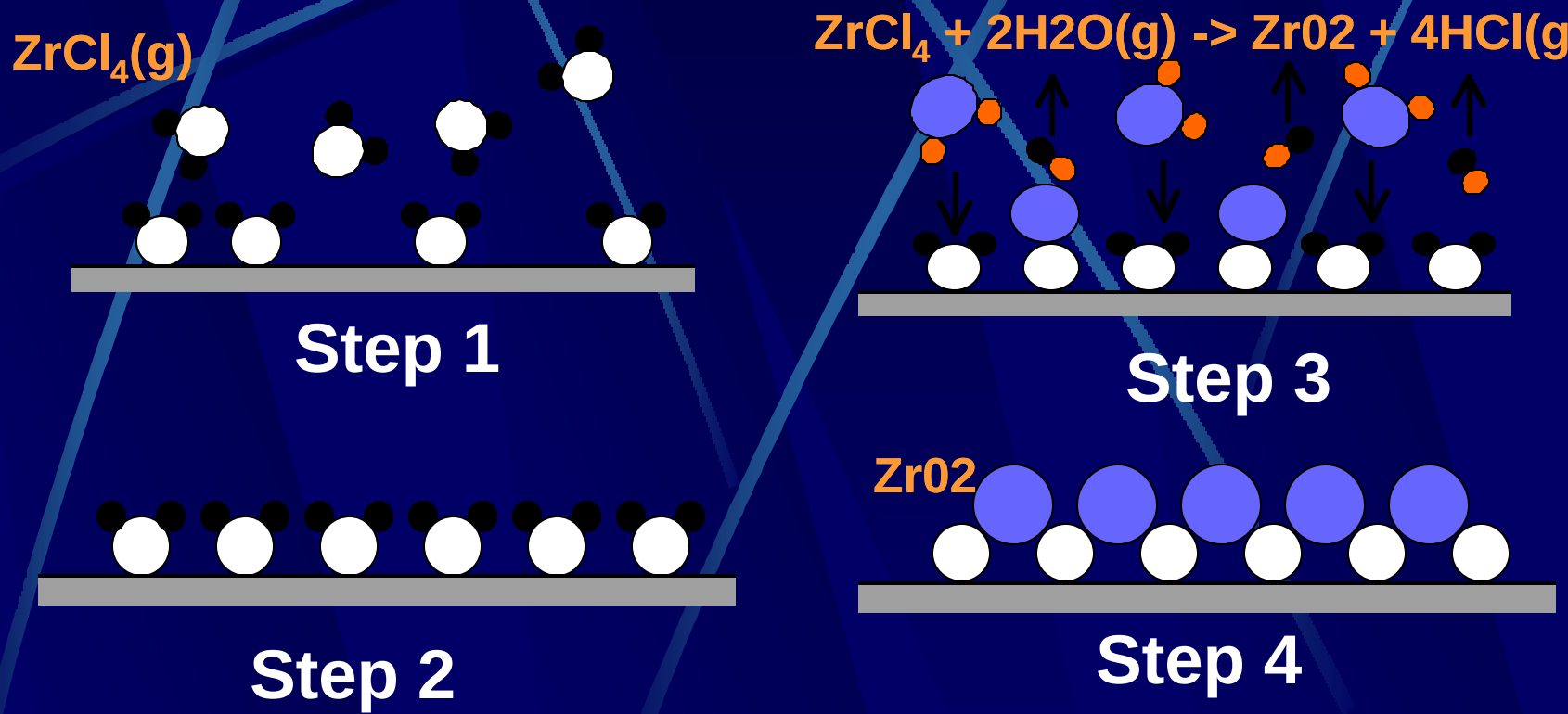
Gate Oxides as Thin as Atoms



What happens when the gate oxide reaches zero?

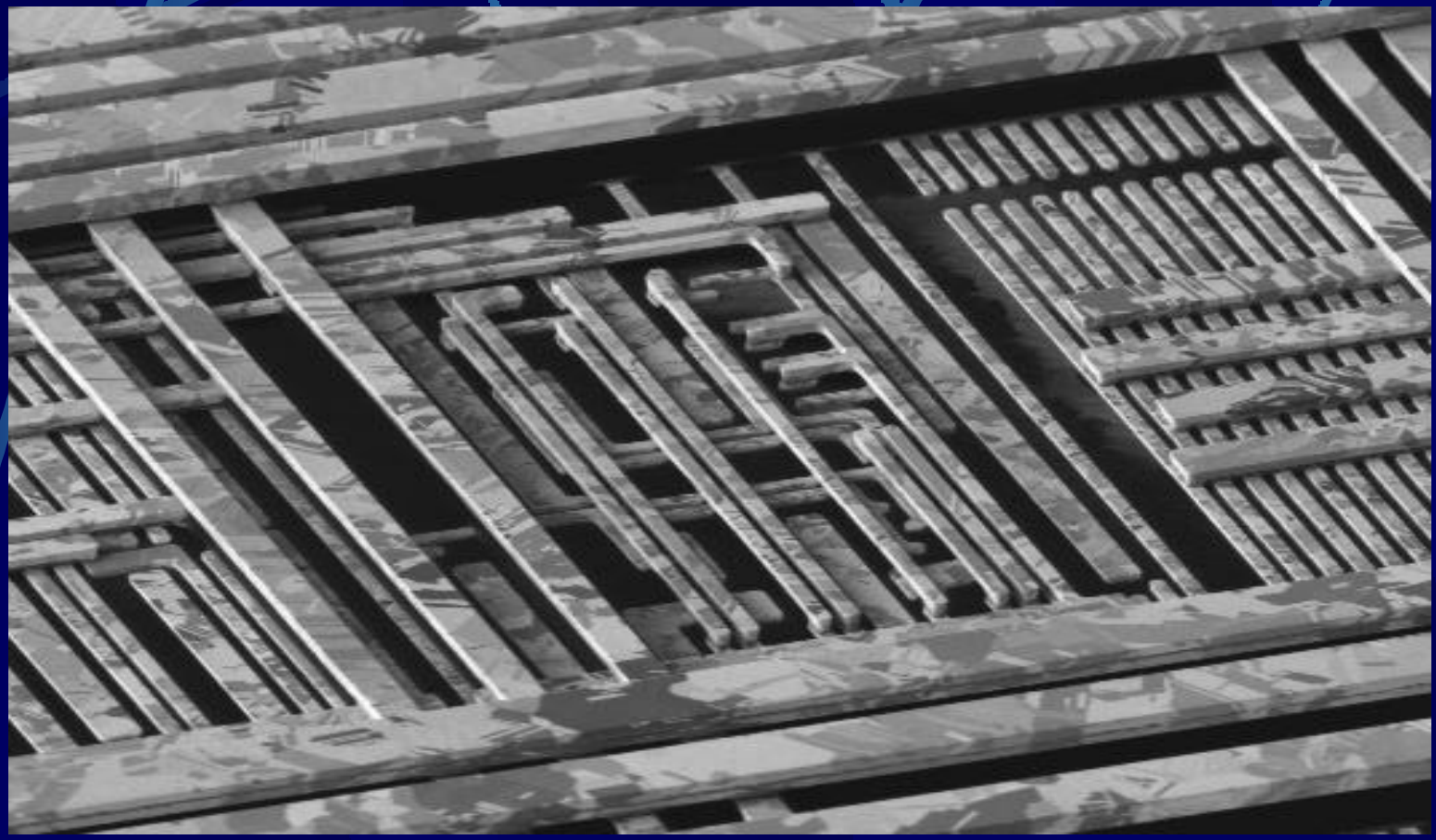
- Switch to high K gate dielectrics
  - –High dielectric constant
  - –Thicker gate = same capacitance
  - –Thicker gate = 1E5 less leakage!
- Silicon industry founded on ability to grow high quality Silicon Dioxide
  - –Need to invent new technologies

High-K Gate Dielectric Formed Using Atomic Layer Chemical Layer Deposition



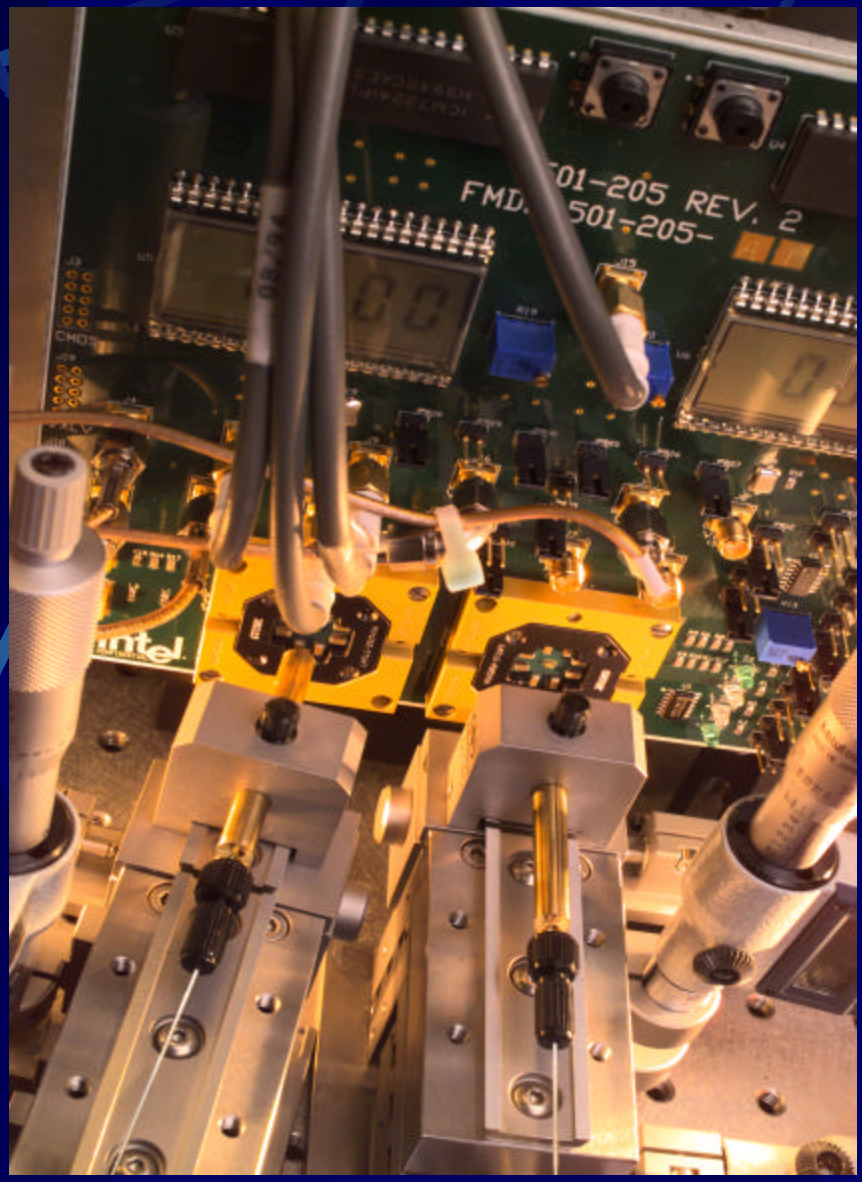
- Sequential introduction of precursors ZrCl4(g), H2O(g)
- Surface reaction between substrate & each precursor until saturation

Copper is in manufacturing



What's beyond Copper?

Early work on Optical Interconnects



What are we going to do with all these transistors?

Multi-Modal Human Interface
Beyond Keyboard and Mouse

Wireless Speech-Driven Earphone

Wireless Digital Pen

Voice / Speech Activation

AV and Pen-Enabled IA Tablet

Media Infrastructure Merging Video, Audio, Graphics and Internet

Computer Vision

Intel Research

- We still have not found a fundamental barrier to extending Moore's law
- We're putting the most advanced technologies into consumer products
- Ronler Acres campus gives us a unique environment
  - Research - Development -Manufacturing

Questions?

See our WEBsite

WWW.Intel.com/research/silicon

Or

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